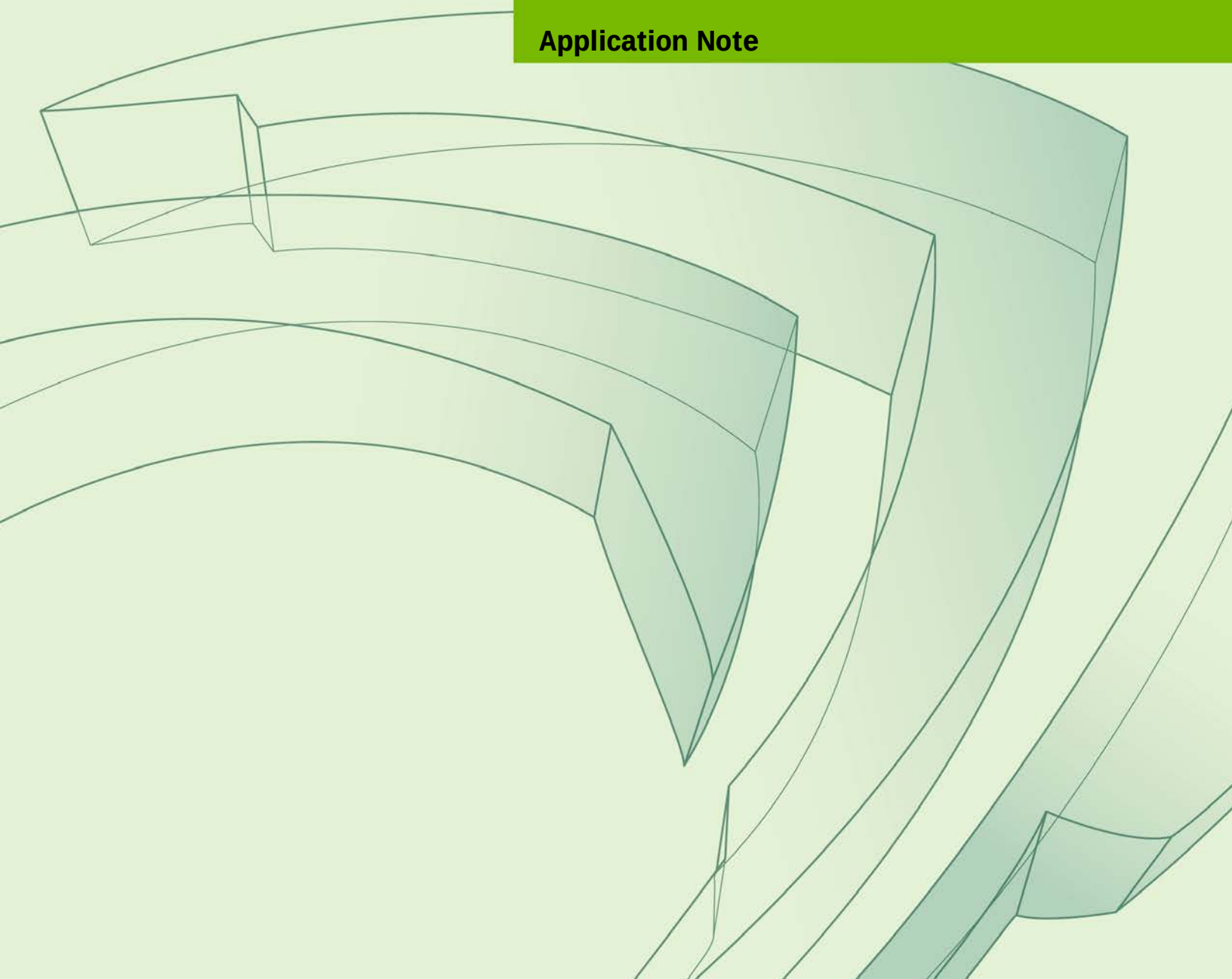
NVIDIA JETSON TX2 AND JETSON TX2i COMPARISON AND MIGRATION

DA-08765-001_v1.4 | March 2018

Application Note



DOCUMENT CHANGE HISTORY

DA-08765-001_v1.4

Version	Date	Description of Change
0.9	Sep 6, 2017	Advanced Draft
1.0	October 24, 2017	General updates throughout this application note
1.1	December 11, 2017	•Updated Table 1 •Voltage range for Jetson TX2i changed to 9V - 19.0V •Added “Auto Power-On Option” section •Updated Figure 3 and Figure 4
1.2	December 21, 2017	•Updated Figure 2, Figure 3, and Figure 4 •Updated Table 1
1.3	March 7, 2018	•Updated Figure 2 and Figure 5 •Removed Jetson TX1 reference
1.4	March 27, 2018	Updated Figure 5

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

This application note compares the features and interfaces supported on the NVIDIA® Jetson™ TX2 and Jetson TX2i modules as well as mechanical differences. This application note also describes the migration path for designers intending to design a carrier board that will support both, with either the same common functionality or be able to take advantage of the features supported on only one or the other module.

Notes: The Jetson TX2i module is suitable for industrial environments.

Jetson TX2 and Jetson TX2i utilize NVIDIA® Tegra® X2 which is a Parker series SoC.

The Jetson TX2 and Jetson TX2i modules are pin compatible with a few exceptions described in this application note. There are also additional differences that need to be considered when designing a new carrier board to support Jetson TX2i alone, or if both modules are to be supported.

The following figures show the Jetson TX2 and Jetson TX2i block diagrams. The items highlighted in **red** are different between the two modules. All the significant interface differences will be described later in this application note.

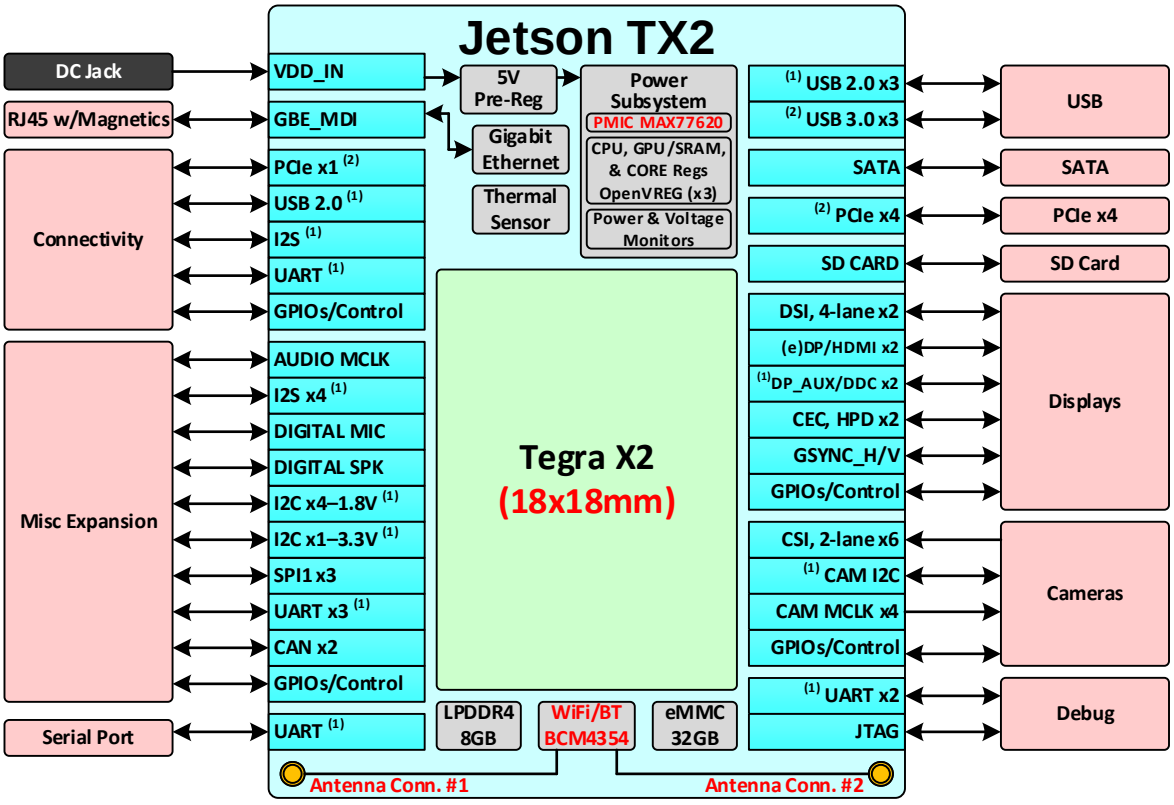


Figure 1. Jetson TX2 Block Diagram

Notes:

1. Some interfaces are shown in multiple locations. There are a total of 4x I2S, 6x I2C (including **DP_AUX/DDC** and **CAM_I2C**), 3x UART, and 3x USB 2.0.
2. USB 3.0, PCIe, and SATA share lanes. Not all instances shown in Figure 1 can be brought out together.

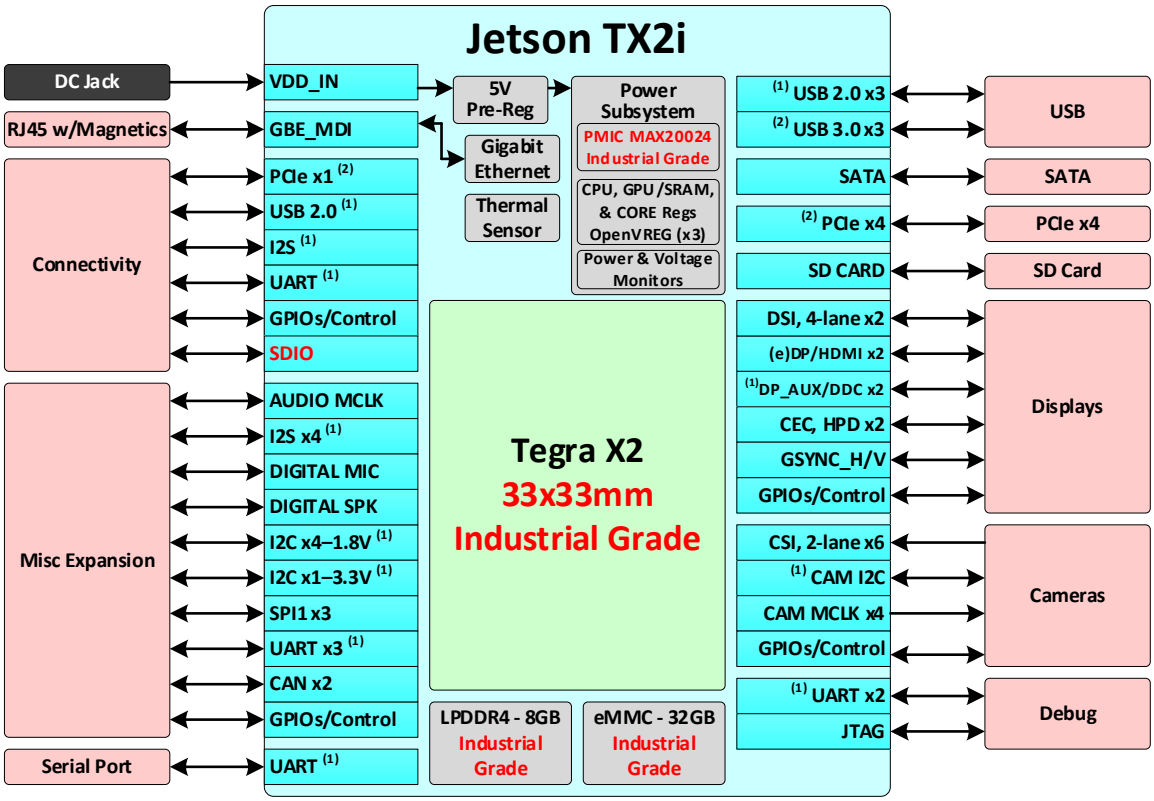


Figure 2. Jetson TX2i Block Diagram

Notes:

1. Some interfaces are shown in multiple locations. There are a total of 4x I2S, 8x I2C (including **DP_AUX/DDC** and **CAM_I2C**), 5x UART, and 3x USB 2.0.
2. USB 3.0, and PCIe, share lanes. Not all instances shown in Figure 2 can be brought out together. See the USB 3.0, PCIe, and SATA lane mapping configuration tables in the "USB 3.0, PCIe, and SATA Mapping" section.
3. Additional components not shown in Figure 2 have been changed to industrial grade.

Table 1 lists the various features & interfaces that are supported on either the Jetson TX2 or the Jetson TX2i module.

Table 1. Differences between Jetson TX2 and Jetson TX2i

Feature	Jetson TX2	Jetson TX2i
LPDDR4	8 GB, 1866 MHz Commercial Grade	8 GB, 1600 MHz Industrial Grade with ECC
DRAM ECC	Not Supported	Supported (SEC-DED)
eMMC	32 GB Commercial Grade	32GB Industrial Grade
PMIC	MAX77620	MAX20024 Industrial Grade
Input Voltage	5.5V to 19.6V	9V to 19.0V
SDMMC	Single Interface (SD Card or SDIO)	Dual Interfaces (SD Card and SDIO)
Wireless	BCM4354 on module	No on-module solution
VIN Monitor	Comparator monitoring **VDD_IN** with output to **SOC_THERM** on Tegra X2	Supervisor monitors **VDD_IN** and drives **VIN_PWR_BAD#** low if **VDD_IN** not valid.
(B49)	**RSVD**	**MOD_PWR_CFG_ID**
(B48)	**RSVD**	**SYS_WAKE#:** Connects to Tegra X2 **GPIO_SYS_4** pin for Power button interrupt and SC7 wake.
Auto-Power-On	Supported by tying **CHARGER_PRSNT#** to **GND**	Supported by leaving **POWER_BTN#** pin **NC** (Pull-up on module brings signal high, resulting in power-on due to PMIC level sensitive on input)

Note: To ensure reliable operation over extended lifetime, the Tegra SoC in Jetson TX2i operates at higher voltages which may result in higher power consumption compared to Jetson TX2

Table 2 (included in the *Jetson TX2/TX2i OEM Product Design Guide*), shows the main module connector pinout with pin and interface differences highlighted.

Table 2. Module Connector (8x50) Pinout Matrix

	A	B	C	D	E	F	G	H
1	VDD_IN	VDD_IN	VDD_IN	RSVD	FORCE_RECOV#	AUDIO_MCLK	I2S0_SDIN	I2S0_LRCLK
2	VDD_IN	VDD_IN	VDD_IN	RSVD	SLEEP#	GPIO19_AUD_RST	I2S0_CLK	I2S0_SDOUT
3	GND	GND	GND	RSVD	SPI0_CLK	SPI0_CS0#	GND	GPIO20_AUD_INT
4	GND	GND	GND	RSVD	SPI0_MISO	SPI0_MOSI	DSPK_OUT_CLK	DSPK_OUT_DAT
5	RSVD	RSVD	RSVD	UART7_RX	I2S3_SDIN	I2S3_LRCLK	I2S2_CLK	I2S2_LRCLK
6	I2C_PM_CLK	I2C_PM_DAT	I2C_CAM_CLK	I2C_CAM_DAT	I2S3_CLK	I2S3_SDOUT	I2S2_SDIN	I2S2_SDOUT
7	CHARGING#	CARRIER_STBY#	BATLOW#	GPIO5_CAM_ FLASH_EN	CAM2_MCLK	GPIO1_CAM1_ PWR#	GPIO4_CAM_ STROBE	GPIO3_CAM1_ RST#
8	GPIO14_AP_WAKE _MDM	VIN_PWR_BAD#	BATT_OC	UART7_TX	CAM_VSYNC	CAM1_MCLK	GPIO0_CAM0_ PWR#	GPIO2_CAM0_ RST#
9	GPIO15_AP2MDM_ READY	GPIO17_MDM2AP_ READY	WDT_TIME_OUT	UART1_TX	UART1_RTS#	CAM0_MCLK	UART3_CTS#	UART3_RX
10	GPIO16_MDM_ WAKE_AP	GPIO18_MDM_ COLDBOOT	I2C_GP2_DAT	UART1_RX	UART1_CTS#	GND	UART3_RTS#	UART3_TX
11	JTAG_GP1	JTAG_TCK	I2C_GP2_CLK	RSVD	RSVD	RSVD	UART0_RTS#	UART0_CTS#
12	JTAG_TMS	JTAG_TDI	I2C_GP3_CLK	RSVD	RSVD	RSVD	UART0_RX	UART0_TX
13	JTAG_TDO	JTAG_GP0	I2C_GP3_DAT	I2S1_LRCLK	SPI1_CS1#	SPI1_MOSI	SPI1_CLK	GPIO8_ALS_PROX_ INT
14	JTAG_RTCK	GND	I2S1_SDIN	I2S1_SDOUT	SPI1_CS0#	SPI1_MISO	GPIO9_MOTION_ INT	SPI2_CLK
15	UART2_CTS#	UART2_RX	I2S1_CLK	I2C_GP0_DAT	I2C_GP0_CLK	GND	SPI2_MOSI	SPI2_MISO
16	UART2_RTS#	UART2_TX	FAN_PWM	AO_DMIC_IN_DAT	AO_DMIC_IN_CLK	SPI2_CS1#	SPI2_CS0#	SDCARD_PWR_EN
17	USB0_EN_OC#	FAN_TACH	CAN1_STBY	CAN1_RX	RSVD	SDCARD_CD#	GND	SDCARD_D1
18	USB1_EN_OC#	RSVD	CAN1_TX	CAN0_RX	CAN0_ERR	SDCARD_D3	SDCARD_CLK	SDCARD_D0
19	RSVD	GPIO11_AP_WAKE _BT	CAN1_ERR	CAN0_TX	GND	SDCARD_D2	SDCARD_CMD	GND
20	I2C_GP1_DAT	GPIO10_WIFI_ WAKE_AP	CAN_WAKE	GND	CSI5_D1-	SDCARD_WP	GND	CSI4_D1-
21	I2C_GP1_CLK	GPIO12_BT_EN	GND	CSI5_CLK-	CSI5_D1+	GND	CSI4_CLK-	CSI4_D1+
22	GPIO_EXP1_INT	GPIO13_BT_WAKE _AP	CSI5_D0-	CSI5_CLK+	GND	CSI4_D0-	CSI4_CLK+	GND
23	GPIO_EXP0_INT	GPIO7_TOUCH_ RST	CSI5_D0+	GND	CSI3_D1-	CSI4_D0+	GND	CSI2_D1-
24	LCD1_BKLT1_PWM	TOUCH_CLK	GND	CSI3_CLK-	CSI3_D1+	GND	CSI2_CLK-	CSI2_D1+
25	LCD_TE	GPIO6_TOUCH_ INT	CSI3_D0-	CSI3_CLK+	GND	CSI2_D0-	CSI2_CLK+	GND
26	GSYNC_HSYNC	LCD_VDD_EN	CSI3_D0+	GND	CSI1_D1-	CSI2_D0+	GND	CSI0_D1-
27	GSYNC_VSYNC	LCD0_BKLT_PWM	GND	CSI1_CLK-	CSI1_D1+	GND	CSI0_CLK-	CSI0_D1+
28	GND	LCD_BKLT_EN	CSI1_D0-	CSI1_CLK+	GND	CSI0_D0-	CSI0_CLK+	GND
29	SDIO_RST#	SDIO_CMD	CSI1_D0+	GND	DSI3_D1+	CSI0_D0+	GND	DSI2_D1+
30	SDIO_D3	SDIO_CLK	GND	DSI3_CLK+	DSI3_D1-	GND	DSI2_CLK+	DSI2_D1-
31	SDIO_D2	GND	DSI3_D0+	DSI3_CLK–	GND	DSI2_D0+	DSI2_CLK-	GND
32	SDIO_D1	SDIO_D0	DSI3_D0-	GND	DSI1_D1+	DSI2_D0-	GND	DSI0_D1+
33	DP1_HPD	HDMI_CEC	GND	DSI1_CLK+	DSI1_D1-	GND	DSI0_CLK+	DSI0_D1-
34	DP1_AUX_CH-	DP0_AUX_CH-	DSI1_D0+	DSI1_CLK–	GND	DSI0_D0+	DSI0_CLK-	GND
35	DP1_AUX_CH+	DP0_AUX_CH+	DSI1_D0-	GND	DP1_TX3-	DSI0_D0-	GND	DP0_TX3-
36	USB0_OTG_ID	DP0_HPD	GND	DP1_TX2-	DP1_TX3+	GND	DP0_TX2-	DP0_TX3+
37	GND	USB0_VBUS_DET	DP1_TX1-	DP1_TX2+	GND	DP0_TX1-	DP0_TX2+	GND
38	USB1_D+	GND	DP1_TX1+	GND	DP1_TX0-	DP0_TX1+	GND	DP0_TX0-
39	USB1_D-	USB0_D+	GND	PEX_RFU_TX+	DP1_TX0+	GND	PEX_RFU_RX+	DP0_TX0+
40	GND	USB0_D-	PEX2_TX+	PEX_RFU_TX-	GND	PEX2_RX+	PEX_RFU_RX-	GND
41	PEX2_REFCLK+	GND	PEX2_TX-	GND	PEX1_TX+	PEX2_RX-	GND	PEX1_RX+
42	PEX2_REFCLK –	USB2_D+	GND	USB_SS1_TX+	PEX1_TX-	GND	USB_SS1_RX+	PEX1_RX-
43	GND	USB2_D-	USB_SS0_TX+	USB_SS1_TX-	GND	USB_SS0_RX+	USB_SS1_RX-	GND
44	PEX0_REFCLK+	GND	USB_SS0_TX-	GND	PEX0_TX+	USB_SS0_RX-	GND	PEX0_RX+
45	PEX0_REFCLK-	PEX1_REFCLK+	GND	SATA_TX+	PEX0_TX-	GND	SATA_RX+	PEX0_RX-

	A	B	C	D	E	F	G	H
46	RESET_OUT#	PEX1_REFCLK-	PEX2_CLKREQ#	SATA_TX-	GND	GBE_LINK1000#	SATA_RX-	GND
47	RESET_IN#	GND	PEX1_CLKREQ#	SATA_DEV_SLP	GBE_LINK_ACT#	GBE_MDI1+	GND	GBE_MDI3+
48	CARRIER_PWR_ON	SYS_WAKE#	PEX0_CLKREQ#	PEX_WAKE#	GBE_MDI0+	GBE_MDI1-	GBE_MDI2+	GBE_MDI3-
49	CHARGER_PRSNT#	MOD_PWR_CFG_ID	PEX0_RST#	PEX2_RST#	GBE_MDI0-	GND	GBE_MDI2-	GND
50	VDD_RTC	POWER_BTN#	RSVD	RSVD	PEX1_RST#	GBE_LINK100#	GND	RSVD

Legend	Ground	Power	Not available (RSVD) on TX2 (Available on TX2i)	Reserved	Redefined for TX2i

Note: RSVD (Reserved) pins on the module must be left unconnected.

FUNCTION AND INTERFACE DIFFERENCE DETAILS

ON-MODULE WIRELESS

Jetson TX2i does not include the on-module wireless functionality that was included on Jetson TX2. This allows the SDMMC3 interface on Tegra X2 previously used for on-module Wireless, to be routed to the SDIO pins on the module connector. In addition, the Tegra X2 UART4 pins are routed directly to the module UART3 pins instead of to a multiplexor to select between the on-module Wi-Fi/Bt or module UART3 pins for Jetson TX2.

POWER

Supported VDD_IN Voltage Range

Jetson TX2 supports a **VDD_IN** range from 5.5V to 19.6V. Jetson TX2i has a more restricted range from 9V to 19.0V.

Vin Monitor

Jetson TX2i implements a VIN monitor using a TPS3808 Supervisor to ensure **VDD_IN** is valid. If **VDD_IN** is out of range, the supervisor will assert **VIN_PWR_BAD#**. Jetson TX2 has a voltage comparator (NCS2202) instead, to monitor **VDD_IN.** If **VDD_IN** drops below a threshold, one of the **SOC_THERM** pins is pulled low.

Jetson TX2, and Jetson TX2i Power-on Option Detection

Jetson TX2i uses a different PMIC (MAX20024) than the Jetson TX2 (MAX77620). Due to the PMIC architecture differences, the platform Power-on mechanism will need to change, from Edge to level triggered. This will require the carrier boards to detect whether a Jetson TX2 module or the Jetson TX2i module is installed. A Reserved pin on the connector which is floating on Jetson TX2 will be grounded on the Jetson TX2i as a means to differentiate between the two module types. The module power configuration identification pin (**MOD_PWR_CFG_ID**) resides on the Module Pin B49.

The updated carrier board, designed to support Jetson TX2i as well as Jetson TX2 will include logic that will use the state of the **MOD_PWR_CFG_ID** pin to determine how the P**OWER_BTN#** signal is handled. If the pin is pulled down due to a Jetson TX2i module being installed, the **POWER_BTN#** pin will be driven to a steady high (ON) or low (OFF) state. If the pin is floating as would be the case if a Jetson TX2 module is installed, a momentary pulse will be generated on the **POWER_BTN** pin of the module to initiate a power-on of the module. With either module type, if the system is already powered, a short press of the power button will put the system in sleep mode (software dependent) if the system is "awake," wake the system if in sleep mode, or cause a force power-off if the Power-on button is held low for approximately 8 to 10 seconds.

Note: When Jetson TX2i is used with a P2597 C02 carrier board, the system can be powered on with just a momentary press of the power button (same as the Jetson TX2 with the P2597 B02/B04 carrier boards). If Jetson TX2i is installed in a P2597 B02/B04 carrier board, the system will power on as soon as the main power is connected due to the different PMIC on the Jetson TX2i module which has a level based ON input instead of pulse based. If the power button is pressed, the module and system will power off. The power button cannot be used to put the system in a sleep mode.

Power Interrupt and Sleep Wake

Pin B48 of module connector is **RSVD** on Jetson TX2, but is assigned as a power button interrupt and SC7 wake interrupt. Pin B48 (**SYS_WAKE#**) connects to the Tegra X2 **GPIO_SYS_4** pin on the module.

Auto-Power-On Option

Auto-Power-On allows the system to power on when the main power supply is connected/enabled, without a power button press. This feature can be supported by Jetson TX2 by connecting **CHARGER_PRSNT#** to **GND**. For Jetson TX2i, Auto-Power-On will occur if the **POWER_BTN#** signal is high when the main power is applied. Since there is a pull-up on this signal on the module, the pin can simply be left **NC** (not connected). In this case, the circuitry described in the "Jetson TX2, and Jetson TX2i "Power-on Option Detection" would not be implemented as this would keep the **POWER_BTN#** signal low until a power button press.

MECHANICAL DIFFERENCES

THERMAL TRANSFER PLATE DIFFERENCES

The Jetson TX2i thermal transfer plate (TTP) differs from the Jetson TX2 TTP. The TTP on Jetson TX2i does not have the opening for the wireless antenna since this is not supported on the Jetson TX2i module. In addition, the heat sink mounting pattern holes (4 small threaded holes in square pattern) that are provided on Jetson TX2 are not available on Jetson TX2i. For a Jetson TX2i design, the main mounting holes will need to be used for connecting a heat sink to the TTP.

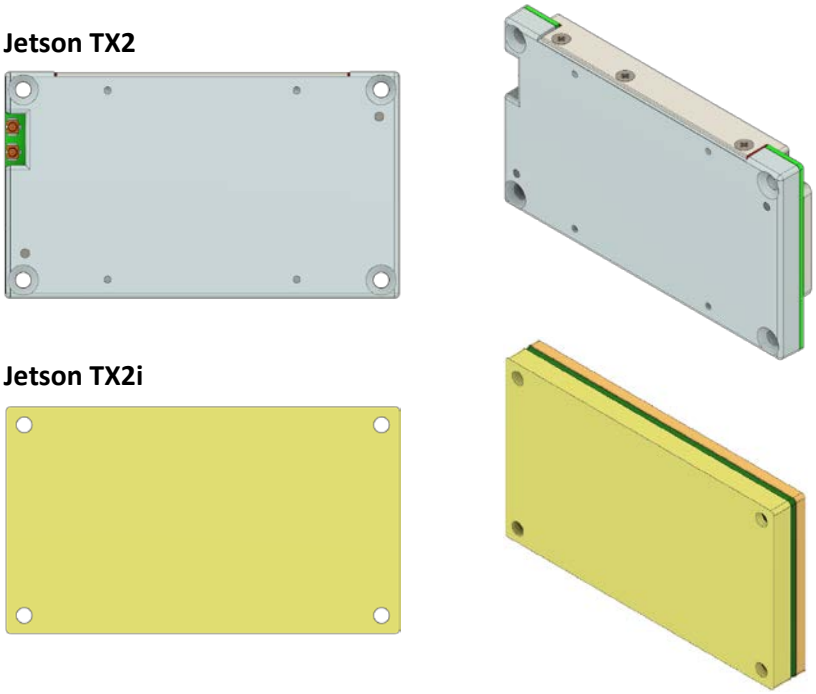


Figure 3. Jetson TX2 and Jetson TX2i Module Top with TTP

BOTTOM STIFFENER DIFFERENCES

The Jetson TX2i bottom stiffener covers more of the PCB compared to the Jetson TX2, including the module mounting hole areas.

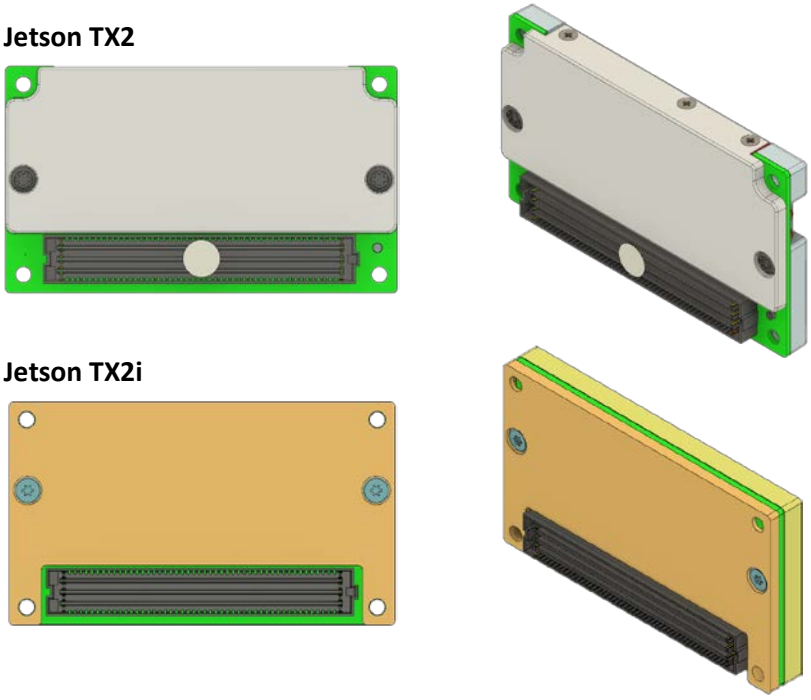


Figure 4. Jetson TX2 and Jetson TX2i Module Bottom with Stiffener

Due to the differences in the bottom stiffener, the standoffs will terminate at the stiffener with Jetson TX2i rather than the PCB as was the case with Jetson TX2. Therefore, the standoff height for Jetson TX2i will be shorter. Going forward, the new carrier board will have an SMT nut on the bottom and either a 7 mm standoff for Jetson TX2 module or a 4 mm standoff for Jetson TX2i. The standoffs have threaded sections that screw into the SMT nuts. See Figure 5 for details.

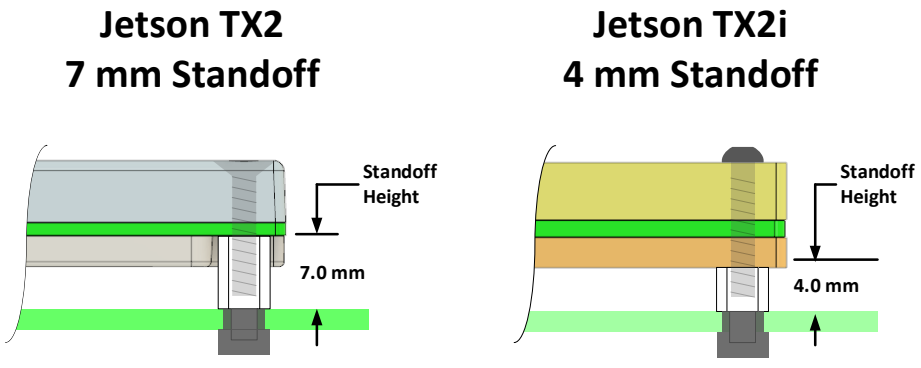


Figure 5. Jetson TX2 and Jetson TX2i Standoff Differences

Notice

The information provided in this specification is believed to be accurate and reliable as of the date provided. However, NVIDIA Corporation (“NVIDIA”) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. NVIDIA shall have no liability for the consequences or use of such information or for any infringement of patents or other rights of third parties that may result from its use. This publication supersedes and replaces all other specifications for the product that may have been previously supplied.

NVIDIA reserves the right to make corrections, modifications, enhancements, improvements, and other changes to this specification, at any time and/or to discontinue any product or service without notice. Customer should obtain the latest relevant specification before placing orders and should verify that such information is current and complete.

NVIDIA products are sold subject to the NVIDIA standard terms and conditions of sale supplied at the time of order acknowledgement, unless otherwise agreed in an individual sales agreement signed by authorized representatives of NVIDIA and customer. NVIDIA hereby expressly objects to applying any customer general terms and conditions with regard to the purchase of the NVIDIA product referenced in this specification.

Unless specifically agreed in writing by NVIDIA, NVIDIA products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of the NVIDIA product can reasonably be expected to result in personal injury, death or property or environmental damage. NVIDIA accepts no liability for inclusion and/or use of NVIDIA products in such equipment or applications and therefore such inclusion and/or use is at customer’s own risk.

NVIDIA makes no representation or warranty that products based on these specifications will be suitable for any specified use without further testing or modification. Testing of all parameters of each product is not necessarily performed by NVIDIA. It is customer’s sole responsibility to ensure the product is suitable and fit for the application planned by customer and to do the necessary testing for the application in order to avoid a default of the application or the product. Weaknesses in customer’s product designs may affect the quality and reliability of the NVIDIA product and may result in additional or different conditions and/or requirements beyond those contained in this specification. NVIDIA does not accept any liability related to any default, damage, costs or problem which may be based on or attributable to: (i) the use of the NVIDIA product in any manner that is contrary to this specification, or (ii) customer product designs.

No license, either expressed or implied, is granted under any NVIDIA patent right, copyright, or other NVIDIA intellectual property right under this specification. Information published by NVIDIA regarding third-party products or services does not constitute a license from NVIDIA to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property rights of the third party, or a license from NVIDIA under the patents or other intellectual property rights of NVIDIA. Reproduction of information in this specification is permissible only if reproduction is approved by NVIDIA in writing, is reproduced without alteration, and is accompanied by all associated conditions, limitations, and notices.

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, “MATERIALS”) ARE BEING PROVIDED “AS IS.” NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE. Notwithstanding any damages that customer might incur for any reason whatsoever, NVIDIA’s aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the NVIDIA terms and conditions of sale for the product.

VESA DisplayPort

DisplayPort and DisplayPort Compliance Logo, DisplayPort Compliance Logo for Dual-mode Sources, and DisplayPort Compliance Logo for Active Cables are trademarks owned by the Video Electronics Standards Association in the United States and other countries.

HDMI

HDMI, the HDMI logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC.

ARM

RM, AMBA and ARM Powered are registered trademarks of ARM Limited. Cortex, MPCore and Mali are trademarks of ARM Limited. All other brands or product names are the property of their respective holders. "ARM" is used to represent ARM Holdings plc; its operating company ARM Limited; and the regional subsidiaries ARM Inc.; ARM KK; ARM Korea Limited.; ARM Taiwan Limited; ARM France SAS; ARM Consulting (Shanghai) Co. Ltd.; ARM Germany GmbH; ARM Embedded Technologies Pvt. Ltd.; ARM Norway, AS and ARM Sweden AB.

Trademarks

NVIDIA, the NVIDIA logo, Jetson, and Tegra are trademarks and/or registered trademarks of NVIDIA Corporation in the U.S. and other countries. Other company and product names may be trademarks of the respective companies with which they are associated.

Copyright

© 2017, 2018 NVIDIA Corporation. All rights reserved.